THAT WHICH IS CLAIMED IS:

1. A time-slot interchange switch, comprising:

an internal frame alignment measurement and programming circuit that determines and stores a first frame offset associated with a first multi-frame data stream received by said switch in a frame offset register, and at least temporarily retains data that identifies presence of an unacceptable frame offset in the internal frame offset register.

2. The switch of Claim 1, wherein said internal frame alignment measurement and programming circuit comprises an error code register that retains the data; and wherein the data is accessible by a user.

3. The switch of Claim 1, wherein said internal frame alignment measurement and programming circuit comprises:

an internal frame alignment counter that determines a first frame delay associated with the first multi-frame data stream; and

an internal frame delay conversion circuit that converts the first frame delay into the first frame offset.

4. The switch of Claim 2, wherein said internal frame alignment measurement and programming circuit comprises:

an internal frame alignment counter that determines a first frame delay associated with the first multi-frame data stream; and

an internal frame delay conversion circuit that converts the first frame delay into the first frame offset.

5. The switch of Claim 4, wherein said frame offset register retains the first frame offset at a first location therein; and wherein said error code register retains a pointer having a value that indicates whether an unacceptable frame offset is present at the first location.

6. The switch of Claim 2, wherein said frame offset register retains the first frame offset at a first location therein; and wherein said error code register retains a pointer having a value that indicates whether an unacceptable frame offset is present at the first location.

7. The switch of Claim 6, wherein said frame offset register retains M rows of frame offset data with N frame offset bytes per row; wherein said error code register retains an M-bit error code; and wherein each bit in the M-bit error code identifies whether at least one of the N frame offset bytes at a corresponding row in said frame offset register is an unacceptable frame offset.

8. The switch of Claim 7, wherein said frame offset register retains nxM rows of frame offset data with N frame offset bytes per row, where n is a nonzero integer; wherein said error code register retains an M-bit error code; and wherein each bit in the M-bit error code identifies whether at least one of the N frame offset bytes at a corresponding row or rows in said frame offset register is an unacceptable frame offset.

9. The switch of Claim 4, wherein said switch is responsive to a clock signal; and wherein said internal frame alignment counter generates an error signal if the first frame delay is not less than a threshold number of cycles of the clock signal.

10. The switch of Claim 9, wherein said internal frame alignment measurement and programming circuit comprises:

a temporary register that receives frame offsets from said internal frame delay conversion circuit; and

an error control circuit that provides an unacceptable frame offset to said temporary register and is responsive to the error signal.

11. The switch of Claim 10, wherein said internal frame alignment measurement and programming circuit comprises:

a frame offset register control circuit that writes the unacceptable frame offset from said temporary register into said frame offset register.

12. The switch of Claim 11, wherein said error control circuit generates the data that is received by said error code register.

13. A time-slot interchange switch, comprising:

an internal frame alignment measurement and programming circuit that determines and then stores a plurality of acceptable frame offsets associated with a first plurality of multi-frame data streams received by said switch and determines and then stores an unacceptable frame offset associated with a multi-frame data stream having an offset that exceeds a maximum offset rating of said switch.

14. The switch of Claim 13, wherein the plurality of acceptable frame offsets and the unacceptable frame offset are stored within a frame offset register.

15. The switch of Claim 14, wherein said internal frame alignment measurement and programming circuit retains user accessible data that identifies presence of the unacceptable frame offset in the internal frame offset register.

16. A time-slot interchange switch, comprising:

a first storage device that is disposed internal to said switch and retains frame delay/offset bytes, with each of the frame offset/delay bytes identifying a frame delay or frame offset associated with a respective multi-frame data stream received by said switch; and

a second storage device that is disposed internal to said switch and at least temporarily retains data that identifies presence of an unacceptable frame delay/offset within said first storage device.

17. The switch of Claim 16, wherein the data identifies presence and location of the unacceptable frame delay/offset within said first storage device.

18. The switch of Claim 16, wherein said first storage device is a register having M rows of storage units therein; and wherein said second storage device retains an M-bit error code therein.

19. A time-slot interchange switch, comprising:

a frame alignment counter that determines a respective frame delay for each of a plurality of multi-frame data streams received by said switch and generates an error signal if any of the frame delays is excessive;

a frame delay conversion circuit that converts the frame delays to acceptable frame offsets;

an error control circuit that generates an error code and an unacceptable frame offset and is responsive to the error signal;

a temporary register that stores the acceptable frame offsets and the unacceptable frame offset received from said frame delay conversion circuit and said error control circuit, respectively;

a frame offset register

a control circuit that writes the acceptable frame offsets and the unacceptable frame offset from said temporary register to a row within said frame offset register; and

an error control register that stores the error code.

20. The switch of Claim 19, wherein the error signal is a carry signal; wherein the error code is an M-bit error code; wherein said frame offset register has M rows therein; and wherein each bit of the M-bit error code within said error control register identifies whether an unacceptable frame offset is stored within a respective row of said frame offset register.

21. A time slot interchange switch, comprising:

an internal frame alignment measurement circuit that determines a first frame offset associated with a first multi-frame data stream received by said switch;

an internal frame offset register that retains the first frame offset at a first location therein; and

an internal error code register that retains a pointer having a value that indicates whether an unacceptable frame offset is present in said internal frame offset register.

22. The switch of Claim 21, wherein said internal frame alignment measurement circuit comprises:

a counter that determines a first frame delay associated with the first multi-frame data stream; and

an internal frame delay conversion circuit that converts the first frame delay into the first frame offset.

23. A method of operating a time slot interchange switch, comprising the steps of:

measuring a first frame offset associated with a first multi-frame data stream received by the switch and then storing the measured first frame offset as an acceptable or unacceptable frame offset in a frame offset register; and

generating, internal to the switch, user accessible data that identifies presence of an unacceptable frame offset in the frame offset register.

24. The method of Claim 23, wherein said generating step comprises generating the user accessible data as an error code that is retained within an error code register.

25. The method of Claim 24, wherein said generating step is followed by the steps of:

measuring a first frame delay associated with the first multi-frame data stream as a multi-bit frame delay; and

writing the multi-bit frame delay into the error code register with the multi-bit frame delay.

26. The method of Claim 25, wherein a number of bits in the multi-bit frame delay is greater than the number of bits in the first frame offset.